REMARKS

Claims 1 and 3-10 are pending in this application. By this Amendment, claim 2 is canceled, claim 1 is amended to incorporate the features of claim 2, claim 7 is amended because of the incorporation of claim 2 into claim 1, claim 3 is amended for clarity, claim 10 is added, and claim 1 is amended to even more clearly distinguish over the applied references. The amendments are supported in the specification by at least page 2, lines 16-22, and page 8, lines 13-18, and Fig. 3B. Claims 8-9 have been withdrawn by the Examiner.

The Office Action rejects claim 3 under 35 U.S.C. §112, first paragraph, because of enablement. By this Amendment, claim 3 is amended for clarity, incorporating the Examiner's helpful suggestion at page 3 of the Office Action. Accordingly, it is respectfully requested that the rejection be withdrawn.

The Office Action rejects claims 1, 2 and 4 under 35 U.S.C. §102(e) over Cohen (U.S. Patent No. 6,774,015); claims 3 and 7 under 35 U.S.C. §102(e) or, in the alternative, 35 U.S.C. §103(a) over Cohen, claim 5 under 35 U.S.C. §103(a) over Cohen in view of Ma (U.S. Patent No. 6,200,866); and claim 6 under 35 U.S.C. §103(a) over Cohen in view of Sugawara (U.S. Patent No. 6,750,486). The rejections are respecfully traversed.

The applied references, alone or in combination, fail to disclose a method of manufacturing a semiconductor device involving an annealing process without performing ion implantation in a single crystal silicon layer and a strain-inducing semiconductor layer, as recited in independent claim 1. Cohen discloses the use of ion implantation to create a strained silicon layer. See Cohen at col. 5, lines 8-12. The injection of high concentrations of ions causes a large extent of damage to the strained silicon layer, and the method recited in independent claim 1 is directed at the formation of strained silicon layers that are damaged only to a small extent. See the specification at page, lines 16-22. Furthermore, the annealing process disclosed in the specification and recited in claim 1 does not involve ion

implantation. See the specification at page 8, lines 4-22 and Figs. 3A and 3B. Cohen therefore fails to disclose the formation of a strained silicon layer without the use of ion implantation. Ma and Sugawara fail to remedy this deficiency of Cohen.

Accordingly, it is respectfully requested the rejections be withdrawn.

With regard to independent claim 10, the applied references, individually or together, fail to disclose a method of manufacturing a semiconductor device involving the cutting of a Si-Si bond of a single crystal silicon layer through providing an annealing process and matching a lattice of the single crystal silicon layer with a lattice of a strain-inducing semiconductor layer.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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Attachment:
Petition for Extension of Time

Date: March 9, 2006

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